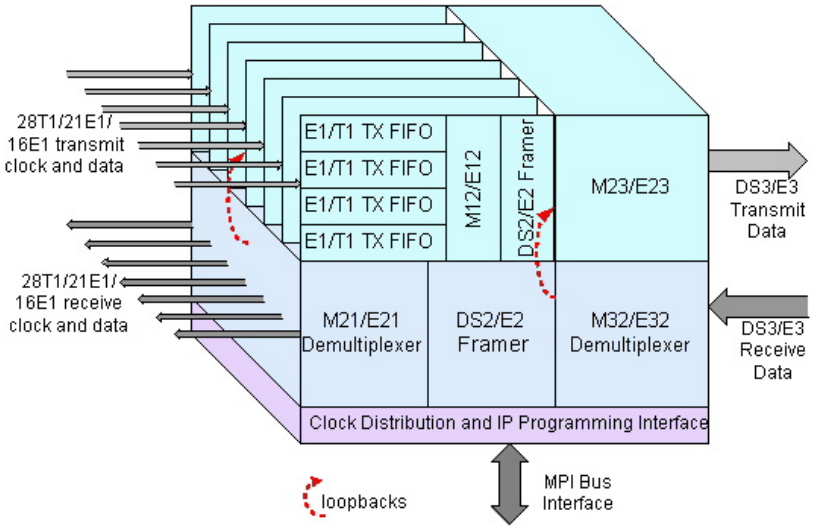
# M13 Multiplexer and Demultiplexer (M13MD)

Product Brief




M13MD Block Diagram

## Overview

The SMD103, M13 Multiplexer and De-multiplexer (M13MD), Intellectual Property (IP) block performs the functions of M13 multiplexing in the transmit direction and M13 de-multiplexing in the receive direction. The purpose of the M13 multiplexer/transmitter is to generate DS3 or E3 data channel running at 44.184 Mb/s or 34.368 Mb/s by multiplexing 28 DS1 or 21 E1 signals, respectively. Conversely, M13 de-multiplexer/receiver generates 28 DS1 or 21 E1 signals out of single DS3 signal. The Silicomotive's M13 Multiplexer and De-multiplexer (M13MD) IP block combines the above functions and it adheres to the recommendations specified in ANSI T1.107, ITU-T G.747 and ITU-T G.751 standards.

The M13MD can be used to multiplex and de-multiplex DS1, DS3 signals in the North American digital telephony hierarchy and E1, E3 signals in the European digital telephony hierarchy. Extensive diagnostic features are also provided.

The IP block operates in one of two available modes. Each operating mode is selected via register programming. Each mode is distinct and mutually exclusive, i.e., the M13MD can only operate in one mode at any given time. The two modes are:

- M13 : Two stage multiplexing/de-multiplexing is implemented. Four DS1 or three E1 signals can be multiplexed/de-multiplexed into/from one DS2 signal. Seven such DS2 signals are multiplexed/de-multiplexed into/from one DS3 signal.
- E13 : Two stage multiplexing/de-multiplexing is implemented. Sixteen E1 signals are multiplexed/de-multiplexed into/from four E2 signals which are then multiplexed/de-multiplexed into/from one E3 signal.

## General Features

- 28 independent DS1 clock inputs each with programmable clock edge adapter.
- 28 independent DS1 outputs each with programmable clock edge adapter.
- 7 independent DS2 framers supporting DS1 and G.747.
- 4 independent E2 framers.
- Supports M23 or C-bit parity formats.
- Supports G.747 formats for E1 to be multiplexed into a DS3.
- Interrupts can be generated on alarm events or status changes.
- Supports DS3 Activated DS2 Line Loopback.
- Supports DS2 Activated DS1 Line Loopback.

## M13 Multiplexer/Transmitter Features

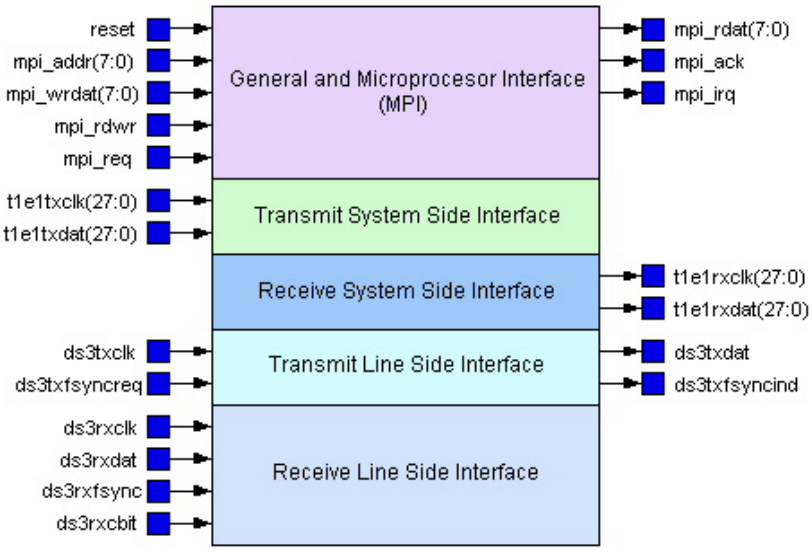
- DS2 insertion of LOS, RAI, AIS and G.747 remote alarm indication via software interface.
- E2 insertion of Remote Alarm Bit, National Use Bit, AIS and LOS.
- Software controlled inversion of second and fourth DS1 streams per ANSI T1.107.
- Insertion of DS1 keep alive signals (AIS) via software interface.
- E1 insertion of Remote Alarm Indication and Reserved Bit.

## M13 De-multiplexer/Receiver Features

- DS2/E2 forced re-frame via software command.
- DS2 average re-frame time less than 6 ms for DS1 mapped DS2 and less than 1 ms for E1 mapped DS2 at a BER of $10^{-3}$. E2 average re-frame time per G.742, section 4.2.
- DS2 OOF indication algorithm is selectable between F-bit only or F-bit / M-bit combined.
- Software controlled inversion of second and fourth DS1 streams per ANSI T1.107.
- DS2/E2 AIS detection at a BER of $10^{-3}$.
- DS2/E2 OOF, RAI, LOS and framing error detection and reporting.
- DS2 extraction of DS2 X-bit or G.747 remote alarm bit and indication of far end receive failure.
- E2 reporting of Alarm Indication Bit (bit 11) and National Use Bit (bit 12).
- DS3 M-frame and M-subframe boundary indications.
- Software controlled insertion of DS2 error conditions like framing bit errors, parity errors.
- Software controlled insertion of E2 framing alignment error conditions.

## Interface

M13MD interfaces to DS3/E3 and DS1/E1 data formats in both receive and transmit directions. It also interfaces to the microprocessor through the generic microprocessor interface.




### Transmit System Side Interface

In transmit direction (DS1/E1--> DS3) each of DS1/E1 ports consists of a clock input t1e1txclk(x) and the corresponding data input t1e1txdat(x). This clock is nominally a 1.544 MHz (DS1 mode) or a 2.048 MHz (E1) clock. Data can be sampled on the rising or falling edge of the clock.

### Transmit Line Side Interface

In the transmit direction (DS1/E1--> DS3), DS3/E3 port consists of clock input ds3txclk operating either on the DS3 or E3 rate (44.736MHz or 34.368 MHz, respectively) and corresponding serial data output ds3txdat. Additionally, depending on the mode of operation, either the input ds3txfsyncreq requests externally a desired frame alignment or the output ds3txfsyncind indicates frame alignment based on free running counters inside M13MD.

### Receive System Side Interface

In the receive direction (DS3 --> DS1/E1) each of 28 DS1/E1 ports consists of a clock output t1e1rxclk(x) and the corresponding data output t1e1rxdat(x). The receive clock is nominally a 1.544 MHz (DS1) or a 2.048 MHz (E1) clock. Data can be issued on the rising or falling edge of the clock.

### Receive Line Side Interface

In the receive direction (DS3 --> DS1/E1), receive DS3/E3 serial data stream (ds3rxdat) is sampled by ds3rxclk clock either on rising or falling edge of the ds3rxclk. To facilitate DS3/E3 frame recognition, M13MD receives ds3rxfsync and ds3rxcbit indicator signals pulsing at the M and C-bit locations, respectively.

## Applications

M13MD IP block can be used to develop a single low cost, low power chip solution to address the need of M13 multiplex/de-multiplex functions or it can be used as one of many IP's interconnected in the system on the chip (SoC) application.

Typical applications for the M13MD support channelized DS3 with serial line interfaces on the low speed side. M13MD design allow usage in following systems/devices:

- Terminal Multiplexers with DS1/E1 and HDSL interfaces
- Add Drop Multiplexers (ADM) with DS1 E1 and HDSL interfaces
- Digital Cross Connect devices with DS1 E1 and HDSL interfaces
- Channelized DS3 applications

The Interfaces of M13MD are designed to interface with other components in the system without need for clock tree balancing across the system. This reduces the timing problems in the large SoC devices.

Typical placement of the M13MD block within the system is between DS3 framer and T1/E1 framers.

## Memory Map

M13MD is a highly configurable IP component. There are 5 groups of registers within M13MD memory map occupying a total of 4 kbits of register address space.

## Implementation

M13MD is designed in Verilog and SystemVerilog. SystemVerilog version includes assertions & interface constructs to facilitate easier SoC integration and superior verification methodology.

M13MD is verified using Synopsys VCS verification platform.

M13MD can be obtained with the standard verilog test bench or with M13VIP, an automated VIP with assertions implemented in SystemVerilog. M13VIP is easy to use and provides very high verification coverage without the need of extended simulation run time.

## Gate Count

M13MD can be synthesized into 100,000 equivalent gates in the technologies ranging from 0.35µm to 90nm.



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